Investigation of Future MRAM Technologies

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I. INTRODUCTION

In the coming year, STT-MRAM with magnetic layers exhibiting perpendicular anisotropy (PMA) will be available as low density (256 Mbit) standalone chips, and also as an embedded memory replacing traditional e-flash. This is a significant step forward for MRAM technology, and it means that the specialized tooling (primarily thin-film deposition and magnetic etch) required for MRAM processing is now seeing widespread deployment in 300 mm semiconductor fabs. With this tooling in place, the barrier facing MRAM adoption for other applications is significantly reduced. There are many other technological hurdles, however, that must be met before MRAM will be able to address these applications, In this talk, we present an overview of some emerging MRAM technologies, and discuss the challenges these emerging technologies must overcome prior to any consideration of widespread adoption.

II. HIGH DENSITY MRAM PATTERNING

One obviously enticing future target for MRAM would be providing a non-volatile memory with DRAM-like performance and cost. There are many reasons why reaching such a goal is difficult, one of which is the lack of a proven technology for patterning MRAM bits at a density that will be competitive with that of DRAM. Recently, Toshiba/SK Hynix presented a 4 Gbit MRAM demo with a full pitch of 90 nm [1]. This impressive density is at least 2x away from being competitive with DRAM. We will describe the challenges involved with patterning MRAM to 55 nm full pitch, and share our recent work fabricating MRAM arrays at this density (Fig. 1).

III. SPIN ORBIT TORQUE MRAM

In recent years, new forms of MRAM other than STT-MRAM have become areas of active exploration. Spin-orbit torque MRAM is an interesting alternative to STT-MRAM for applications where endurance and switching speed are crucial. This is because the switching current no longer flows vertically through the magnetic tunnel barrier, but instead travels horizontally in a layer of material underneath the free layer which has a high degree of spin-orbit scattering. (Fig. 2). We will give a short overview of the different materials and magnetic configurations being considered for SOT-MRAM, and share our recent work examining high-speed switching of 3-terminal SOT devices with an in-plane free layer.

IV. VOLTAGE-CONTROLLED MAGNETIC ANISOTROPY

Voltage-controlled magnetic anisotropy could be the basis for an even more efficient form of MRAM. In traditional STT-MRAM, the energy required to switch the bit is orders of magnitude larger than the energy barrier created by the uniaxial magnetic anisotropy in the system. In a high RA tunnel barrier (e.g. 200 Ω−υm^2), applying a bias voltage produces an E-field that can lower the free layer PMA, while flowing negligible current across the tunnel barrier. If the VCMA coefficient is large enough, the PMA can be eliminated, and the magnetization may precess about an in-plane magnetic field provided by an in-stack biasing layer [2]. This is now a "toggle" memory switching system, which requires pre-read, and likely

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write verification, but has the advantages of unlimited endurance, sub-ns write speed, and extremely low power. In order to scale to useful densities, however, the VCMA coefficient needs to be 10-30x larger than the 30 fJ/Vm typically found in CoFeB/MgO tunnel barriers. In this presentation, we will describe how we characterize the VCMA coefficient in experimental film stacks, and share recent results of our exploration of higher VCMA coefficient devices.

REFERENCES

1) S. –W. Chung, et al., " 4Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure", *IEDM Conference* 16-660 (2016).
2) C. Grezes, et al., "Ultra-low switching energy and scaling in electric-field-controlled nanoscale magnetic tunnel junctions with high resistance-area product" *Appl. Phys. Lett*. **108**, 012403 (2016).

ILLUSTRATIONS

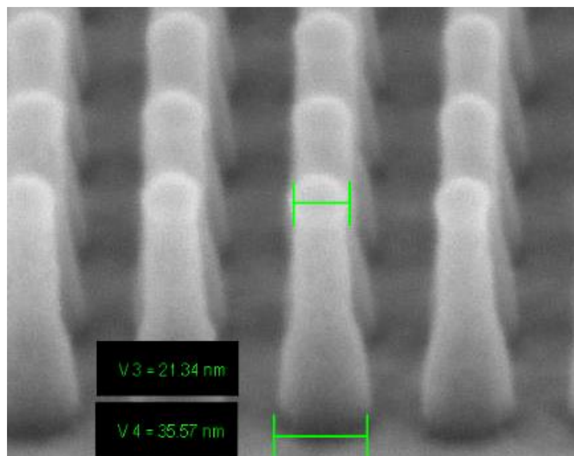

Fig. 1. SEM image of MRAM bits patterned at 55 nm full pitch

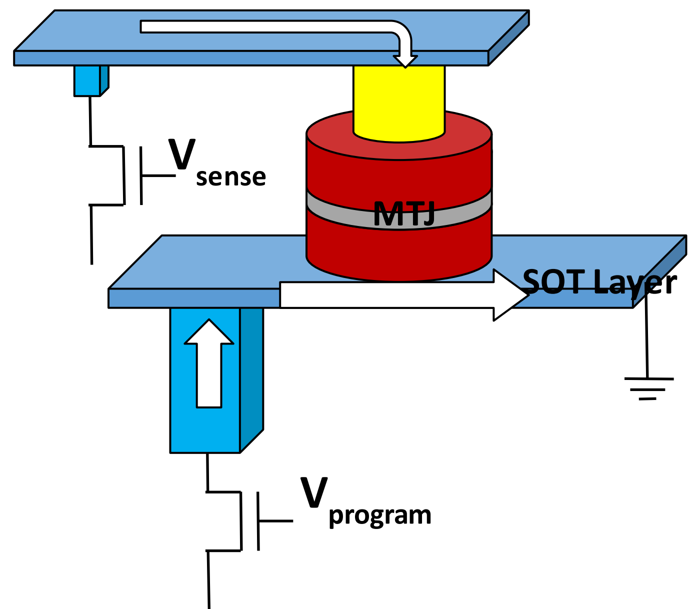

Fig. 2. Schematic of a 3-terminal SOT-MRAM bit.