ULTRAFAST 3-TERMINAL AND 2-TERMINAL MRAM ENABLED BY SPIN-ORBIT TORQUE OR THERMALLY ASSISTED SWITCHING

C. Bi[1], N. Sato[2], R. Cheaito[3], R. M. White[4], M. Asheghi[5], K. E. Goodson[6] and S. X. Wang[7]

[1, 2, 4, 7]Department of Materials Science and Engineering, [2, 7]Department of Electrical Engineering, and [3, 5, 6]Department of Mechanical Engineering, Stanford University, Stanford, CA 94305, USA

[1]cbi@stanford.edu [2]norisatotohoku@gmail.com [3]rcheaito@stanford.edu [4]rmwhite@stanford.edu [5]masheghi@stanford.edu [6]goodson@stanford.edu [7]sxwang@stanford.edu

I. Introduction to STT-MRAM

In MRAM, a current rather than a magnetic field must be used for switching the free layer from the viewpoint of scalability. Conventionally, the applied current passes through the tunnel barrier layer of a MTJ to generate spin-transfer torque (STT) for switching free layer but the write current shares the same path as read current, as shown in **Fig.1**. The large write current passing through the barrier layer will cause aging issues of tunnel barrier, and the shared read and write path also increases the read error ratio of MRAM during read operations, reducing its reliability. In STT-MRAM, an ultrathin tunnel barrier, around 1 nm, must be used to obtain a low resistance-area (RA) product that guarantees enough write current density under the voltage capability of access transistors. On the other side, the ultrathin tunnel barrier layer sharply reduces the perpendicular magnetic anisotropy (PMA) and tunneling magnetoresistance (TMR) of MTJs. The former directly determines the thermal stability of MTJs and thus the minimum dimension of a single MTJ in MRAM; the latter determines the resistance ratio between low and high resistance states and thus read margins of MRAM. Moreover, the ultrathin barrier layer further limits thickness tolerance of the tunnel barrier in manufacturing since any small variation in the barrier thickness can dramatically change MTJ resistance.

II. Three-Terminal SOT-MRAM

An alternative way for switching the free layer is by using an in-plane current-induced spin-orbit torque (SOT) generated at the interface between the free layer and an SOT layer, as shown in **Fig. 1**. The SOT layer consists of materials showing strong spin Hall effects (SHE), such as heavy metals, which can generate strong SOT under an applied in-plane current. In the three-terminal SOT-induced magnetization switching, the large write current does not pass through the tunnel barrier and thus the reliability and endurance are highly improved compared to STT switching. The read operation utilizes an independent current path with a much smaller sensing current to detect MTJ resistance states. The separated read and write paths also reduce the read error ratio, and more importantly, it does not need RA as low as STT-MRAM. This is because the write current passes through highly conducting heavy metal layers, not tunnel barriers, and the critical switching current can be easily satisfied by access transistors. Currently, one main obstacle of three-terminal SOT-MRAM in application is the requirement of an applied in-plane magnetic field for SOT deterministic switching, which leads to the scaling problem. The comparison of selected metrics of STT-MRAM and SOT-MRAM is given in **Table I**. Notably, sub-ns switching speed has been achieved in SOT-MRAM, making it attractive for applications such as lower level cache, traditionally the domain of SRAM.

III. Two-Terminal SOT-MRAM

Although the three-terminal SOT-MRAM has many advantages as discussed above and may also facilitate to integrate SOT devices into present logic circuits or cache memory, two-terminal SOT devices are also attractive for high-density memory application because of a much smaller cell size. Similar to STT-MRAM as shown in **Fig. 1**, the two-terminal SOT device has a very thin and narrow heavy metal underlayer so that an in-plane current can also be generated when applying an out-of-plane current. The generated in-plane current creates SOT and further switches the free layer of a MTJ.

To achieve a larger in-plane current through the heavy metal underlayer, a thinner underlayer is preferred, but on the other side, the thinner underlayer will reduce SOT efficiency when the thickness is comparable

Shan X. Wang
E-mail: sxwang@stanford.edu
tel: +1-650-723-8671

with the spin diffusion length of the underlayer (typically several nm). Therefore, choosing a proper thickness of the underlayer is very important to get a high switching efficiency.

In this work the demonstration of two-terminal SOT switching was achieved in a MTJ structure by using Ta as the underlayer. **Fig. 2.** shows the out-of-plane current induced MTJ switching under an in-plane field. Like a three-terminal SOT switching device, the opposite switching direction for a positive and a negative in-plane field was observed, indicating a SOT dominated MTJ switching since STT switching direction does not relate to the in-plane field direction. Without applied in-plane magnetic fields, the MTJ can be switched due to STT (data not shown). We will also present the trade-off between 3- and 2-terminal SOT-MRAM designs and the outlook of emerging topological materials for enhanced SOT-based switching.

III. Ultrafast MRAM with Thermally Assisted Switching

As a comparison to the 2-terminal SOT device, we will also discuss another path to ultrafast operation of MRAM, which can be realized by the thermally-assisted switching mechanism. We experimentally determine the thermal conductance in ultrathin MgO and interface thermal conductance at CoFeB-MgO interface by using the pico-second time-domain thermoreflectance technique. Our experimental data enables the accurate simulation of temperature profile in magnetic tunnel junctions, which is critical to designing a thermally assisted MRAM cell.

REFERENCES

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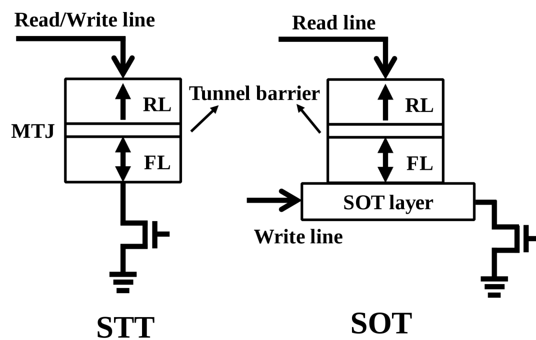

Fig.1 Schematic of STT (left) and SOT (right) memory cell. RL: reference layer; FL: free layer.

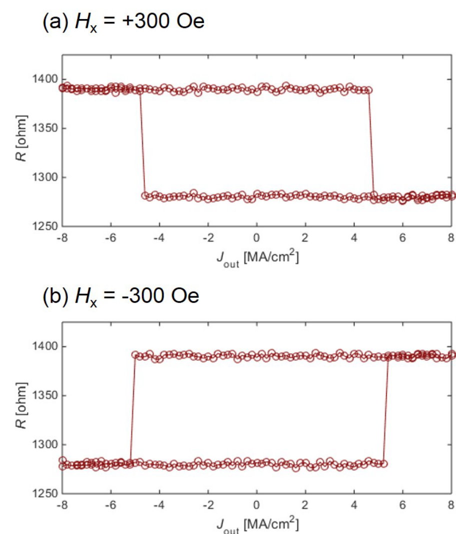

Fig.2 Switching of a 2-terminal SOT device under (a) positive field or (b) negative field along the x-axis (same as the in-plane current).

Table I Representative parameters for STT-MRAM and SOT-MRAM.

	RA (Ω•μm^2)	Switching current density (A/cm^2)	Switching time (ns)	External magnetic field (Oe)	References
STT-MRAM	< 9	3×10^6	2 - 10	0	(Wang *et al.* 2018) [1]
SOT-MRAM	Depends on 3-Terminal or 2-Terminal	5.4×10^6	0.18 – 0.4	50-1000 or zero	(Garello *et al.* 2014) [2]