DEVELOPMENT OF PERPENDICULAR STT-MRAM FOR LAST LEVEL CACHE APPLICATIONS

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I. STT-MRAM FOR EMBEDDED APPLICATIONS

Perpendicular Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) technology has overcome major hurdles over the past few years, opening the way to mass production for embedded non-volatile memory applications. The first major advance needed to enable embedded applications was the demonstration that the Magnetic Tunnel Junction (MTJ) devices can withstand backend-of-line (BEOL) processes at 400°C without degradation of their magnetic and electrical transport properties. Since we first reached this milestone in 2013 [1, 2], significant progress has been made, as shown by the demonstration of perpendicular magnetic anisotropy (PMA) exceeding 10 kOe for sub-30nm devices submitted to 2.5 hours annealing after patterning [3].

Another key milestone was the demonstration of Mb-sized fully functional chips having ppm-level defect rate and error-free writing and reading [2]. This achievement also enabled the thorough investigation of data retention at the ppm-level error rate required for applications. By measuring the retention error rate as a function of bake temperature and duration, we have shown that data retention in the ppm regime is given by an effective thermal stability factor, which depends both on the median and standard deviation of the thermal stability factor distribution [4]. Most importantly, the effective thermal stability factor is strongly dependent on temperature. It exhibits an almost linear decrease over a wide range of temperatures, with a variation coefficient as high as 0.45 per degree for standard MTJ stacks [4, 5]. Thus, meeting data retention targets at high operating temperature (e.g at least 150°C for automotive applications) requires much higher values at room temperature. However, since STT write current is also proportional to the thermal stability factor, such devices also become harder to write.

II.STT-MRAM FOR FLASH REPLACEMENT APPLICATIONS

The first mainstream embedded application for STT-MRAM is for embedded Flash replacement for 2X lithography nodes, at which the fabrication process of conventional embedded Flash is complex and expensive. For many of these applications, data written in the memory must be preserved during the reflow soldering process used to package the chips. This entails heating the chips at 260°C for up to 90 seconds. As discussed above, because of the strong temperature dependence of the thermal stability factor, meeting this requirement is more challenging than achieving 10 years data retention with ppm error rate at 150°C. We have designed a MTJ stack with high PMA and low temperature coefficient of the thermal stability factor to qualify STT-MRAM for reflow soldering. As shown in Fig. 1a, the error rate of 30 chips after simulated reflow procedure remains below the 10 ppm target, low enough to be handled by ECC. The write error rate at room temperature of one of these 10 Mb chips is shown in Fig. 1b for 250 ns long write pulses. Without ECC, error-free writing is achieved with significant margin. This demonstrates that reflow qualification is achieved without compromising chip performance [6, 7].

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III.TOWARD LAST LEVEL CACHE APPLICATIONS

STT-MRAM is also an attractive candidate to replace SRAM for Last Level Cache (LLC) memory applications at advanced lithography nodes. Indeed, the 1Transistor-1MTJ STT-MRAM cell is much more compact than the standard 6 transistors SRAM cell. As reported previously [8] and shown in Fig. 2, STT-MRAM devices can be written reliably down to sub-ns write pulses by overdriving. However, voltages used in this example are too high. For STT-MRAM to provide a viable alternative to SRAM in terms of density and performance, sub-30 nm MTJ devices operating at low write current and voltage and high read/write speed are needed. This poses a new set of materials and physics challenges in terms of spin-torque efficiency, tunnel transport properties, as well as tight control of distributions and process-induced damage. We have developed ultralow power and voltage devices compatible with LLC applications at 0X nodes [9]. In this presentation, we will discuss development of materials, devices and processes underlying this breakthrough.

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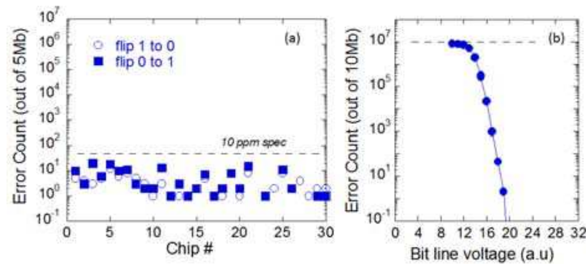

Fig.1 (a) Error count of 30 different 10Mb chips after simulated reflow soldering procedure (90 seconds bake at 260°C). The chips are initialized in two 5 Mb blocks of logic 0 and 1. Solid and open symbols show bit flips from 0 to 1 and 1 to 0, respectively. (b) Error count as a function of bit line voltage for one of the chips shown in (a). All bit can be written without any error, without ECC, using 250ns write pulses.

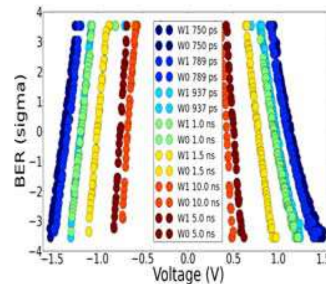

Fig.2 Error rate vs. write pulse voltage and length for a single device (reproduced from [8]).