PERPENDICULAR MAGNETIC TUNNEL JUNCTION ARRAY PROCESSING FOR STT-MRAM

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I. INTRODUCTION

While the physics of STT-MRAM and perpendicular magnetic tunnel junction (pMTJ) devices are well understood, the processing of these devices has been more of an art for many years, primarily developed in the HDD industry. Basic processing requirements such as thin film stack thickness and composition control, as well as repeatable etching of non-volatile materials in dense arrays are extremely challenging and have been among the major impediments for widespread adaptation of STT-MRAM. Some of recent developments in the process equipment at Applied Materials addressing these issues are reviewed in this talk [1-4].

II. MTJ FILM STACK DEPOSITION

Specialized chambers and new processes have been developed to deposit the MTJ film stack [1]. In Endura Clover™ PVD System of Applied Materials, a multi-cathode chamber was developed using the targets in a tilted geometry to the wafer normal and including wafer rotation (Fig. 1 left). This allows controlling thickness and uniformity of ultra-thin films. A RF sputtering chamber was specially designed for MgO tunnel barrier that allows good barrier integrity, stoichiometry, and particle control. High vacuum at 10^{-9} Torr was implemented for all chambers as well as the platform to keep materials and their interfaces free of moisture. In-situ heating and cooling processes have also been developed and integrated with the PVD system for texture control. In addition, in-situ process control tools are being developed such as in-situ film thickness measurement and automatic

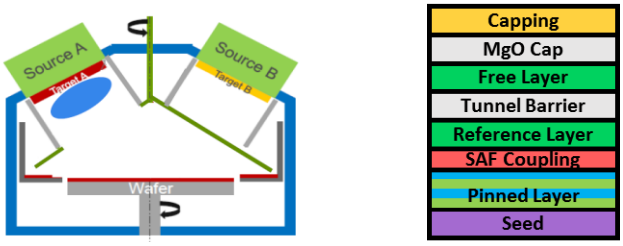

Fig. 1. (left) Multi-cathode chamber schematic. (right) pMTJ stack structure.

FL material stack and process, for interface controlled PMA, were optimized to improve switching efficiency [3]. To get low switching voltage (Vc) at the same data retention energy barrier (Δ = Eb/kT), FL needs to have low magnetic moment, low damping, and high exchange stiffness. As shown in Fig. 2, by optimizing from FL1, FL2 achieved lower Ic (94 vs. 126 μA) with the same $\Delta \sim 70$.

The tunnel barrier is another critical part of the MTJ stack. The MgO tunnel barrier can be deposited by RF sputtering of MgO target or by DC sputtering of Mg and oxidizing the film. Devices with MgO made by both methods were fabricated and measured. Fig. 3 inset shows device by both methods have TMR ~ 125% and Rp around 6500 Ohm with film RA ~ 10 Ohm·μm^2. Although resistance and TMR are similar for the two types of devices, the breakdown voltage (V_{BD}) differentiates them with V_{BD} = 1550 mV for RF MgO and V_{BD} = 1410 mV for Mg plus oxidation as shown in Fig. 3. RF MgO demonstrated better barrier integrity than Mg plus oxidation thus more suitable for tunnel barrier with RA around 5 ~ 10 Ohm·μm^2. In order to reduce particles for RF MgO process, special attention was given to chamber design and chamber conditioning.

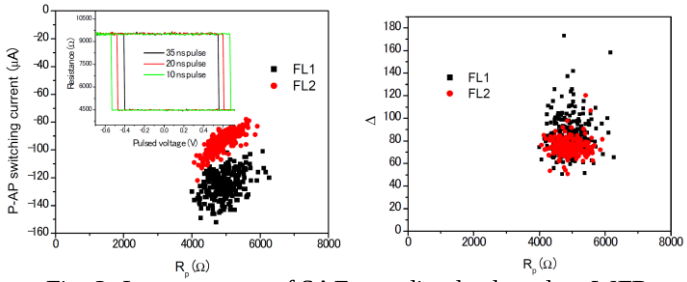

Fig. 2. Improvement of SAF coupling leads to low WER.

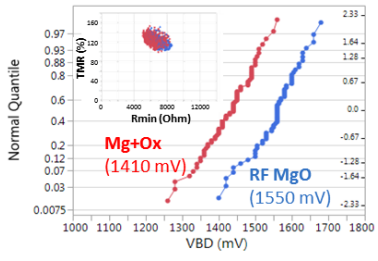

Fig. 3. V_{BD} between RF MgO and Mg+Ox.

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III. MTJ PATTERNING

MTJ patterning and etching is critical step that controls short yields and performance degradation. Traditional halogen based reactive ion etch (RIE) is not very effective in providing high yielding MTJ arrays because of performance degradation induced by chemical damage. In addition, the MTJ pillar hard mask patterning step is also critical for yields and has to be carefully optimized along with the MTJ etch process to get to memory densities that are competitive to semiconductor memories.

MTJ etch was developed using plasma ribbon beam etching (PRBE) tool of Applied Materials (Fig. 4 left) [4]. The noble-gas plasma ribbon beam was generated in a remote inductively-coupled-plasma radio-frequency source with ions accelerated by a pulsed DC system. A ribbon beam was formed using novel extraction optics that resulted in constant distance from the plasma source for each point along the ribbon. The wafer was rotated during ribbon beam processing to achieve superior uniformity, and optical emission spectroscopy was used for precise endpoint control. With PRBE, each MTJ pillar across the 300 mm wafer saw the same beam density and beam angle distribution.

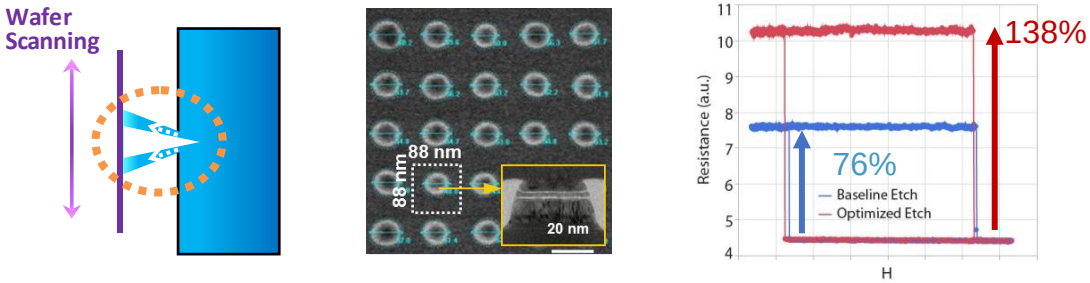

Fig. 4. (left) DRBE schematic. (middle) An MTJ array processed by DRBE. (right) Process optimization to improve TMR after patterning.

Fig. 4 middle shows Top-down SEM and cross-section TEM image of a MTJ array processed by DRBE. The MTJ CD is around 40 nm, and array pitch is 88 nm (~4Gb of MTJs per die). MTJ etch process was optimized to get higher TMR of 138% compared to 76% by baseline etch with film TMR = 160% at RA = 5 Ohm·μm^2 annealed at 400°C for 0.5 hour (Fig. 4 right). TMR% and Hc data down to 25nm CD MTJ was shown in a previous publication [4] using this technique, that demonstrated damage free etch is possible with this technique.

IV. CONCLUSIONS

We have discussed recent developments in equipment and process for STT-MRAM, where MTJ film stack deposition is directly related to device performance, and MTJ etch affects MTJ array scaling towards small CDs and tight pitches. With the device physics well studied, these key processes would be the enablers of STT-MRAM for applications such as embedded memory and cache memory.

REFERENCES

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2) M. Pakala, et al., IMW 2018
3) C. Park, et al., IEDM 2015, pp 664-667
4) L. Xue, et al., IEEE Trans. Magn. 51, 4401503 (2015)