ACCELERATION TESTS FOR DATA RETENTION AND ENDURANCE IN STT-MRAM

S. IKEGAWA, F. MANCOFF, H.-J. CHIA, J. SUN, K. NAGEL, J. JANESKY, S. DESHPANDE, M. DEHERRERA, H. K. LEE, A. DEMIRAY, S. KARRE, T. ANDRE, S. M. ALAM, AND S. AGGARWAL

Everspin Technologies, Inc., Chandler, Arizona, USA

I. INTRODUCTION

Magnetoresistive Random Access Memory (MRAM) is the memory of choice for persistent memory applications. From data centers to edge devices, data processing demands and evolution in computing drive the growing need for MRAM. It is a reliable persistent memory device with high speed, high endurance, and power saving ability. Field-switched MRAM has been in volume production at Everspin since 2006 in densities up to 16Mb. Spin-transfer torque (STT) MRAM enables smaller magnetic tunnel junction (MTJ) devices for higher densities. A 64Mb DDR3 MRAM product based on in-plane STT switching was first developed at Everspin [1]. This technology was transferred to its foundry partner, GLOBALFOUNDRIES. Everspin is in volume production at GLOBALFOUNDRIES for a 256Mb DDR3 STT-MRAM standalone part using perpendicular MTJ (pMTJ) devices [2].

The key characteristics of STT-MRAM are high data retention and high endurance compared with other emerging non-volatile memory technologies. To enable reasonable learning cycle times, it is essential that we develop methodologies to evaluate these devices in significantly shorter durations than their product retention and endurance specifications. Therefore, we use accelerated tests, in which one environmental parameter is changed from the normal operation condition to enhance the error rate. However, conducting short-time wafer tests to assess long-life product reliability can be a challenging process. This paper attempts to address this challenge with the following approach. The first step is to define the acceleration parameter. The second step is to understand any side effects of the acceleration tests. The next step is to define test patterns that reflects how the memory will be used. Last but not the least is to account for the distribution in performance. The above approach can help define a path from MTJ development to successful STT-MRAM product and an overview of STT-MRAM reliability.

II. RESULTS AND DISCUSSION

To predict data retention and endurance life times, we need to test under acceleration conditions, such as high temperature and high voltage. For data retention (DR) in in-plane MTJs, magnetic field can be used as an acceleration parameter to measure a value of the energy barrier to thermal reversal (E_b); time-dependent coercivity from field sweep measurements or thermal fluctuation broadening of coercivity were used to derive E_b. For pMTJ devices, however, temperature acceleration gives a better indication of the DR performance [3]. Figure 1 shows an example of experimental results for a 256kb test array that was annealed at high temperature, and the number of bits that underwent a thermally-induced reversal was measured after each anneal step. Four different wafers are shown in Fig. 1, and variations in the free layer design for these wafers leads to improving DR from FL1 to FL4. Fitting the data to a thermal activation model gives a mean value of E_b, a bit-to-bit distribution of E_b, and the coupling field ratio (H_{cpl}/H_k). H_{cpl} is the stray magnetic field from the fixed layer to the free layer, which causes a shift of the magnetic hysteresis loop, and H_k is the effective perpendicular anisotropy field of the free layer in an MTJ element. After characterizing at multiple high temperatures and times and then extrapolating to low temperature and long time based on a thermal activation model, we can make a diagram of the retention error rate as a function of temperature and time, as in Figure 2. Thus, we can predict the retention error rate for the chip under operation conditions. In order to predict the endurance performance, voltage acceleration is used in time-dependent dielectric breakdown (TDDB) measurements for the tunnel barrier. It is key to manage the voltage acceleration for MTJ TDDB because of the high current density in these small MTJ elements that

Sumio Ikegawa
E-mail: sumio.ikegawa@everspin.com
tel: +1-480-347-1111

can lead to Joule heating [4].

The acceleration parameters can bring unintended environmental changes to the MTJs, which need to be considered. For example, in an MTJ, H_{cpl}/H_k depends on temperature and a high H_{cpl}/H_k exaggerates the DR error rate at elevated temperatures. During extrapolation from high temperature to the operation temperature, this effect needs to be considered when predicting life times. In TDDB measurements, the voltage acceleration enhances Joule heating in the MTJ. The MgO temperature is much higher in the acceleration test than that in MRAM operation and can greatly affect life time. We need to account for these side effects to effectively deploy acceleration tests.

As we scale to higher densities, bit to bit distributions significantly affect the MRAM chip performance. Therefore, it is critical to evaluate and improve the bit to bit distributions during development. In DR experiments, the slope of BER vs. time in Fig. 1 is a good indication of the E_b distribution. In TDDB endurance measurements, the β value of the Weibull plots represents a distribution of life times among MTJs. These distributions need to be accounted for when defining MTJ requirements for chip performance.

III. SUMMARY

We will present test methodologies deployed to predict data retention and endurance life time using acceleration parameters. Unintended side effects of the acceleration parameters are evaluated and accounted for in the predictions. The combination of these opens a path from MTJ development to successful STT-MRAM product. We would like to acknowledge our foundry partner, GLOBALFOUNDRIES for their support during this project.

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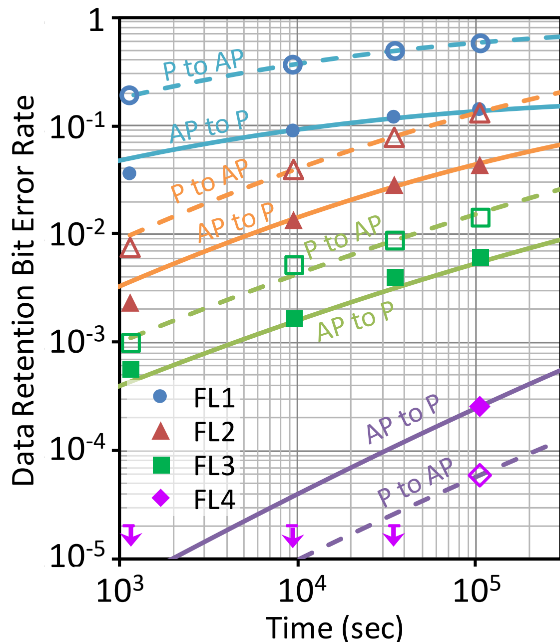

Fig. 1. Thermally-induced reversal rate for four different free layers at 220°C.

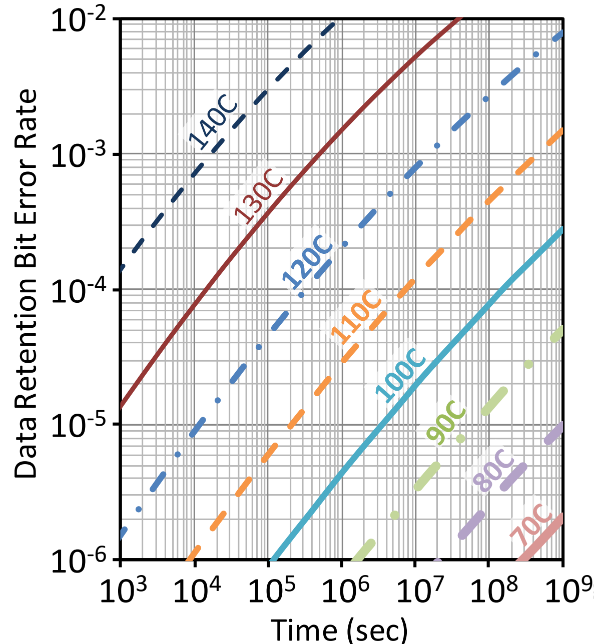

Fig. 2. Expected data retention bit error rate derived from data at multiple temperatures and extrapolation from them.