TIMING RECOVERY FOR LOW-SNR MAGNETIC TAPE RECORDING CHANNELS

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I. INTRODUCTION

The continued commercial success of magnetic tape storage necessitates exponential increases in areal density and cartridge capacity [1] to keep pace with the current exponential growth of data. For a given media and head design point, increasing areal density leads to a higher raw bit-error rate (BER) due to the reduced signal-to-noise ratio (SNR). Increased raw BERs can be handled by improvements in error-correction coding (ECC) schemes [2,3], but low-SNR operating points represent a major challenge to the read channel design. Specifically, timing recovery (TR), which aims to recover the optimum sampling instants for detecting the written data on tape, is a key issue at low SNR: the TR loop suffers from noisy and erroneous timing error estimates due to unreliable bits from the detector, which leads to loss-of-lock (LOL) or cycle-slip events, resulting in very long bursts of bit errors that the ECC scheme cannot handle.

In this work, we propose a new robust TR scheme for low-SNR tape read channels, which fully exploits the parallel-track recording nature of linear tape drives and significantly reduces the LOL rate compared to the conventional 2nd-order phase-locked loop (PLL) approach [4], with only a small increase in implementation complexity. Other schemes based on iterative and/or joint TR & detection/decoding are known to work at low SNR, but are significantly more complex than the proposed scheme.

II. TIMING RECOVERY FOR LOW-SNR TAPE CHANNELS

In state-of-the-art magnetic tape drives, 32 parallel data tracks are written simultaneously onto the magnetic media by means of a write head module with a rigid linear array of write transducers. Similarly, a read head module comprising a linear array of magneto-resistive read elements simultaneously read 32 data tracks. Reading and writing is carried out under closed-loop track-following and skew-following servo control to deal with lateral tape motion and tape skew, as well as reel-to-reel tape transport servo control to minimize tape speed variation. Furthermore, all write (read) elements on a module are driven (sampled) by a common clock.

We propose a new TR scheme which exploits these correlations and constraints within a group of N parallel tracks by means of a geometric model of the array head shown in Fig. 1A for N=4. The dynamics of each read element on the array head is largely determined by two degrees of freedom of the head, where 1) θ_k (and f_k) is a head phase (and frequency) which represent a residual sampling phase offset in the tape transport direction, and 2) ϕ_k (and ω_k) is a head skew (and angular velocity) which represents a residual rotation around the head center. Parameter $d^{(i)}$ denotes the signed distance of the i-th read element from the head center. The total phase offset of the i-th read element (including an optional per-track phase offset $\theta_k^{(i)}$) is then given by $\tau_k^{(i)} = \theta_k + d^{(i)}\phi_k + \theta_k^{(i)}$. Assuming 2nd-order process models for head phase and skew, see Fig. 1B, and by means of Kalman filter theory and some approximations/simplifications, the new TR loop shown in Fig. 2 is derived. Note that the loop filter has grown to a N-input N-output unit, compared to N conventional PLLs operating independently on each track, but the increase in complexity is small.

III. PERFORMANCE RESULTS

To evaluate the performance of the proposed parallel-track TR scheme, we recorded a repeating 255-bit pseudorandom binary sequence (PRBS) at linear densities from 600 kbpi to 775 kbpi in steps of 25kbpi in a commercial tape drive which simultaneously writes and/or reads 32 parallel data tracks. The recorded data was read back using a tape read head with 350nm-wide TMR readers and captured digitally in-drive at 1.25x the baud rate. Groups of N=8 read back signals from parallel tracks are subsequently processed by a software read channel which implements three TR schemes: A) N=8 conventional PLLs, B) a previously described “global frequency” scheme which tracks N=8 channel phase offsets and a single (joint) frequency offset [5], and C) the new proposed TR scheme of Fig. 2 with N=8 tracks. The read channel’s

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interpolated TR loop comprises an interpolation filter, an FIR-based fractional tap-spacing channel equalizer with partial-response class 4 (PR4) target, Mueller-Müller timing error detector (MM-TED) and a configurable loop filters. The MM-TED gets reconstructed PR4 symbols from a symbol-by-symbol detector, while a simple EPR4 sequence detector is used for data bit detection. The stream of detected bits from each track is split into sectors of 8160 bits, which roughly corresponds to a tape codeword-interleave (CWI-4) unit. Groups of eight consecutive bits are mapped into bytes. We declare a LOL in a sector when more than 90% of bytes are in error in a sliding observation window of 50 bytes. The LOL rate is defined as the ratio of the number of sectors with at least one LOL event compared to the total number of sectors.

Figure 3 and Fig. 4 show the LOL rate and the raw BER performance achieved by the proposed new TR scheme operating on N=8 parallel tracks, as well as the conventional PLL and the "global frequency" scheme, as a function of linear recording density. The new TR scheme significantly outperforms the other schemes at high linear densities (low SNR) with no LOL events at linear densities ≤ 750 kbpi. At 775 kbpi, occasional LOL events start occurring with the new TR scheme, compared to more than 50% LOL rate for the two other schemes.

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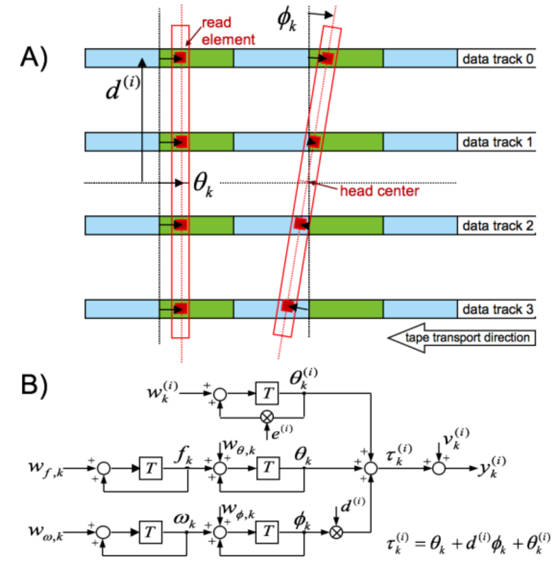

Fig. 1. A) Head array model with phase and skew offsets and B) State-space process model.

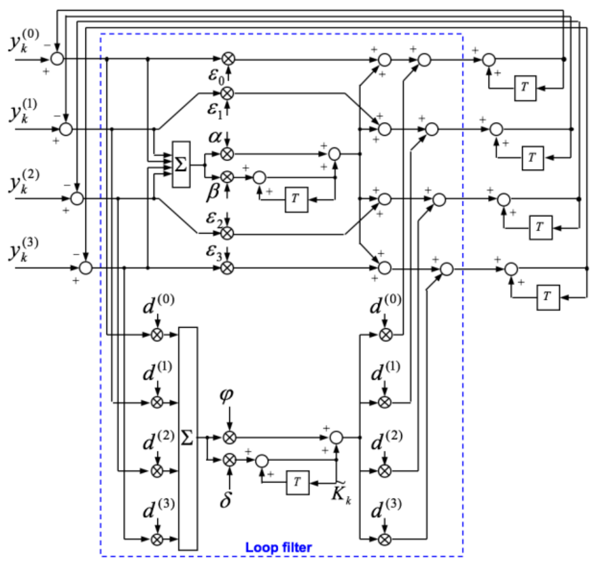

Fig. 2. Model of the proposed timing recovery loop with N-input N-output loop filter (N=4 tracks).

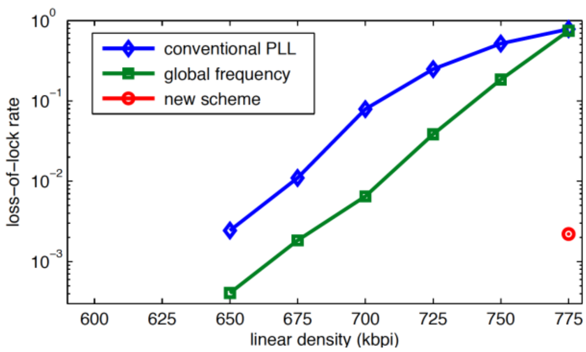

Fig. 3. LOL rate as a function of linear density.

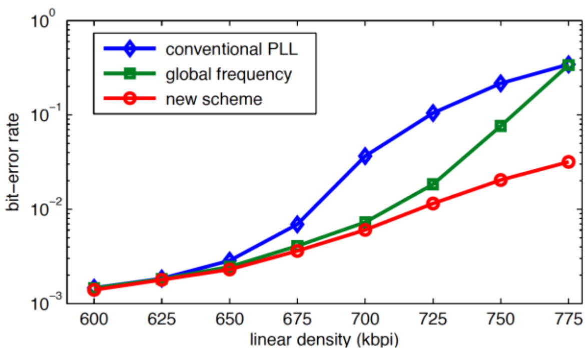

Fig. 4. BER as a function of linear density.